Amendments to the Claims

33. (Currently Amended) An in-plane switching mode liquid crystal display comprising:

gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

data and common electrodes parallel to the data bus line in the pixel region, the data electrodes including a first capacitor portion overlapping the common line and the common electrodes including a second capacitor portion overlapping the common line, the first and second capacitor portions substantially parallel to the gate bus line, ~~having portions~~ for first and second storage capacitors, respectively;

a passivation layer over the thin film transistor and the data electrode, wherein the common electrode is formed on the passivation layer parallel to the data electrode and overlapping the gate and data bus lines; and

a first alignment layer on the common electrode.

34. (Previously Presented) The in-plane switching mode liquid crystal display of claim 33, further comprising a black mask and a color filter on a second substrate opposite to the first substrate.

35. (Previously Presented) The in-plane switching mode liquid crystal display of claim 34, wherein the black mask includes one of a Cr and a CrOx metal layer.

36. (Previously Presented) The in-plane switching mode liquid crystal display of claim 35, wherein the metal layer has a thickness of about 0.1 μm and a width of about 10 μm.

37. (Previously Presented) The in-plane switching mode liquid crystal display of claim 34, further comprising a second alignment layer on the color filter layer.

38. (Previously Presented) The in-plane switching mode liquid crystal display of claim 37, wherein the second alignment layer includes one of polyimide and photo-alignment materials.

39. (Previously Presented) The in-plane switching mode liquid crystal display of claim 34, further comprising a liquid crystal layer between the first and second substrates.

40. (Previously Presented) The in-plane switching mode liquid crystal display of claim 33, further comprising gate, data, and common pads connected to driving circuits.

41. (Previously Presented) The in-plane switching mode liquid crystal display of claim 40, wherein the gate and data bus lines are connected to the driving circuits.

42. (Previously Presented) The in-plane switching mode liquid crystal display of claim 40, wherein the common bus line is grounded through the common pad.

43. (Previously Presented) The in-plane switching mode liquid crystal display of claim 40, wherein the gate, data and common pads include first, second and third metal layers, respectively.

44. (Previously Presented) The in-plane switching mode liquid crystal display of claim 43, wherein the first metal layers includes Mo/Al double metal layers together with the gate electrode and common bus line.

45. (Previously Presented) The in-plane switching mode liquid crystal display of claim 43, wherein the second metal layer includes Cr together with the source and drain electrodes.

46. (Previously Presented) The in-plane switching mode liquid crystal display of claim 43, wherein the third metal layer includes indium tin oxide together with the common electrode.

47. (Previously Presented) The in-plane switching mode liquid crystal display of claim 33, further comprising a grounding wiring connected to the gate and data bus lines through an electrostatic shielding circuit.

48. (Currently Amended) An in-plane switching mode liquid crystal display comprising:

gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

data ~~and common~~ electrodes parallel to the data bus line in the pixel region,

common electrodes including parallel portions substantially parallel to the data bus line and a connecting portion substantially parallel to the gate bus line, the parallel portions extending from the connecting portion and having an oblique side ~~wherein the common electrode has first and second oblique sides~~;

a passivation layer over the thin film transistor and the data electrode; and

a first alignment layer on the common electrode.

49. (Currently Amended) The in-plane switching mode liquid crystal display of claim 48, wherein the ~~first~~ oblique side is inclined counterclockwise to an X axis direction with an angle θ_A.

50. (Currently Amended) The in-plane switching mode liquid crystal display of claim 48, wherein the ~~second~~ oblique side is inclined clockwise to an X axis direction with an angle θ_B.

51. (Previously Presented) The in-plane switching mode liquid crystal display of claim 49, wherein an alignment direction is inclined counterclockwise to an X axis direction with an angle θ_R.

52. (Previously Presented) The in-plane switching mode liquid crystal display of

claim 50, wherein an alignment direction is inclined counterclockwise to an X axis direction with an angle θ_R.

53. (Previously Presented) The in-plane switching mode liquid crystal display of claim 51, wherein the range of θ_R is about 0° to 90°.

54. (Previously Presented) The in-plane switching mode liquid crystal display of claim 52, wherein the range of θ_R is about 0° to 90°.

55. (Previously Presented) The in-plane switching mode liquid crystal display of claim 53, wherein the range of θ_A is about θ_R to 90°.

56. (Previously Presented) The in-plane switching mode liquid crystal display of claim 54, wherein the range of θ_B is about 90°- θ_R to 90°.

57. (Previously Presented) The in-plane switching mode liquid crystal display of claim 49, wherein θ_A is about 45°.

58. (Previously Presented) The in-plane switching mode liquid crystal display of claim 50, wherein θ_B is about 45°.

59. (Previously Presented) The in-plane switching mode liquid crystal display of claim 51, wherein θ_R is about 75°.

60. (Previously Presented) The in-plane switching mode liquid crystal display of claim 52, wherein θ_R is about 75°.

61. (Previously Presented) The in-plane switching mode liquid crystal display of claim 48, wherein the common electrode is formed on the passivation layer.

62. (Previously Presented) The in-plane switching mode liquid crystal display of claim 48, wherein the common electrode overlaps the gate and data bus lines.

63. (Previously Presented) The in-plane switching mode liquid crystal display of claim 48, wherein the data and common electrodes have portions for first and second storage capacitors.

64. (Currently Amended) An in-plane switching mode liquid crystal display comprising:

gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

data and common electrodes parallel to the data bus line in the pixel region, the data electrodes including a first capacitor portion overlapping the common line and the common electrodes including a second capacitor portion overlapping the common line, the first and second capacitor portions substantially parallel to the gate bus line;

a passivation layer over the thin film transistor and the data electrode, wherein the common electrode is formed on the passivation layer parallel to the data electrode;

a light shielding layer on the passivation layer; and

a first alignment layer on the common electrode.

65. (Previously Presented) The in-plane switching mode liquid crystal display of claim 64, wherein the common electrode and the light shielding layer include Mo and indium tin oxide.

66. (Previously Presented) The in-plane switching mode liquid crystal display of claim 65, wherein the thickness of the Mo is about 1000Å.

67. (Currently Amended) ~~The~~ An in-plane switching mode liquid crystal display, comprising: ~~of claim 64,~~

gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

data and common electrodes parallel to the data bus line in the pixel region;

a passivation layer over the thin film transistor and the data electrode, wherein the common electrode is formed on the passivation layer parallel to the data electrode;

a light shielding layer on the passivation layer; and

a first alignment layer on the common electrode,

wherein the light shielding layer overlaps a portion of the gate bus line through a hole in the gate insulator and the passivation layer.

68. (Previously Presented) The in-plane switching mode liquid crystal display of claim 64, wherein the data and common electrodes have portions for first and second storage capacitors.

69. (Currently Amended) An in-plane switching mode liquid crystal display comprising:

gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

data and common electrodes parallel to the data bus line in the pixel region, the data electrodes including a first capacitor portion overlapping the common line and the common electrodes including a second capacitor portion overlapping the common line, the first and second capacitor portions substantially parallel to the gate bus line;

a passivation layer over the thin film transistor and the data electrode, wherein the common electrode is formed on the passivation layer parallel to the data electrode and overlaps the gate and data bus lines;

a light shielding layer on the passivation layer; and

a first alignment layer on the common electrode.

70. (Previously Presented) The in-plane switching mode liquid crystal display of claim 69, wherein the common electrode and the light shielding layer include opaque materials.

71. (Previously Presented) The in-plane switching mode liquid crystal display of claim 69, wherein the data and common electrodes have portions for first and second storage capacitors.

REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The Advisory Action dated May 29, 2003 and the Final Office Action of January 13, 2003 has been received and contents carefully reviewed.

In the Final Office Action, the Examiner rejected claims 33-47, 64-66, and 68-71 under 35 U.S.C. § 103(a) as being unpatentable over the related art shown in Figures 1a and 1b in view of Hebiguchi (U.S. Pat. No. 6,091,473, hereinafter referred to as 'Hebiguchi '473'); rejected claims 48-60, 62, and 63 under 35 U.S.C. § 103(a) as being unpatentable over the related art shown in Figures 1a and 1b in view of Hebiguchi (U.S. Pat. No. 6,137,557, hereinafter referred to as 'Hebiguchi '557'); rejected claim 61 under 35 U.S.C. § 103(a) as being unpatentable over the related art shown in Figures 1a and 1b in view of Hebiguchi '557 and further in view of Hebiguchi '473; and objected to claim 67 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant submits that the rejections set forth in the Final Office Action are moot in view of the amendments set forth herein. Reconsideration of the claims is respectfully requested in view of the foregoing amendments to the claims and the following remarks.

The Examiner is thanked for the indication of allowable subject matter in claim 67. Applicant have amended claim 67 to be in independent form incorporating the limitations of the base claims and any intervening claims. Therefore, Applicant submits that this claim is in condition for allowance.

With respect to independent claim 33, claim 33 and claims 34-47, which ultimately depend therefrom, are allowable over the cited references in that each of these claim recites at least "the data electrodes including a first capacitor portion overlapping the common line and

the common electrodes including a second capacitor portion overlapping the common line, the first and second capacitor portions substantially parallel to the gate bus line." None of the cited references, either singly or in combination, teaches or suggests at least these features of the claimed invention. Therefore, Applicant submits that claim 33, and claims 34-47, which depend therefrom, are allowable over the cited references.

With respect to independent claim 48, claim 48 and claims 49-63, which ultimately depend therefrom, are allowable over the cited references in that each of these claim recites at least "data electrodes parallel to the data bus line in the pixel region, common electrodes including parallel portions substantially parallel to the data bus line and a connecting portion substantially parallel to the gate bus line, the parallel portions extending from the connecting portion and having an oblique side." None of the cited references, either singly or in combination, teaches or suggests at least these features of the claimed invention. Therefore, Applicant submits that claim 48, and claims 49-63, which depend therefrom, are allowable over the cited references.

With respect to independent claim 64, claim 64 and claims 65-66 and 68, which ultimately depend therefrom, are allowable over the cited references in that each of these claim recites at least "data and common electrodes parallel to the data bus line in the pixel region, the data electrodes including a first capacitor portion overlapping the common line and the common electrodes including a second capacitor portion overlapping the common line, the first and second capacitor portions substantially parallel to the gate bus line." None of the cited references, either singly or in combination, teaches or suggests at least these

features of the claimed invention. Therefore, Applicant submits that claim 64, and claims 65-66 and 68, which depend therefrom, are allowable over the cited references.

With respect to independent claim 69, claim 69 and claims 70-71, which ultimately depend therefrom, are allowable over the cited references in that each of these claim recites at least "data and common electrodes parallel to the data bus line in the pixel region, the data electrodes including a first capacitor portion overlapping the common line and the common electrodes including a second capacitor portion overlapping the common line, the first and second capacitor portions substantially parallel to the gate bus line." None of the cited references, either singly or in combination, teaches or suggests at least these features of the claimed invention. Therefore, Applicant submits that claim 69, and claims 70-71, which depend therefrom, are allowable over the cited references.

Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 496-7500.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0911, under Order No. 8733.250.21.00-US. A duplicate copy of this paper is enclosed.

Respectfully submitted,

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Date: October 14, 2003

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